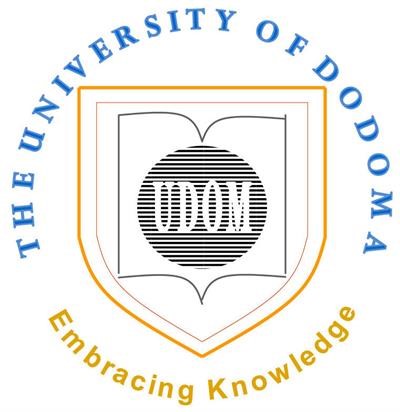
**THE UNIVERSITY OF DODOMA**

**THE COLLEGE OF INFORMATICS AND VIRTUAL EDUCATION**



**Department:** DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

**Course Code**: CT 211

**Course Name:** COMPUTER ORGANIZATION AND ARCHITECTURE

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**Registration number:** T/UDOM/2020/00348

**Task:** Assignment 03

**Assignment 03**

**Question 1.**

Suppose that when Program A is run, the user CPU time is 3 seconds, the elapsed wall-clock time is 4 seconds, and the system performance is 10 MFLOP/sec. Assume that there are no other processes taking any significant amount of time, and the computer is either doing calculations in the CPU, or doing I/O, but it can't do both at the same time. We now replace the processor with one that runs six times faster, but doesn't affect the I/O speed. What will the user CPU time, the wall-clock time, and the MFLOP/sec performance be now?

**Solution**

**Data given**

In program A:

User CPU time = 3seconds

Elapsed wallclock time = 4seconds

System Performance = 10MFLOP/sec

**Required** (after the processor is replaced with the one that runs six times faster)

User CPU time?

Elapsed wall-clock time?

System Performance in MFLOP/sec?

* **User CPU time**

Let the first processor be A and the second one be processor B

**NOTE**: The CPU performance is inversely proportional to the user CPU time that is

CPU performance of processor B/CPU performance of processor A = User CPU time in A/User CPU time in B

But CPU performance of processor B/CPU performance of processor A is 6:1

6=3/User CPU time in B

User CPU time in B = 0.5sec

The user CPU time in B (after the processor being replaced is 0.5seconds

* **Elapsed wall-clock time**

From the question the I/O is not affected by the increase in speed, so the I/O time remains to be 1second whereas the I/O time is the period spent waiting for the I/O operations to be completed. Since the wall-clock time is the actual time taken from the start of the computer program to the end

Wall-clock time = User CPU time + I/O time= 0.5+1 = 1.5seconds

Wall-clock time after the processor being replaced is 1.5seconds

* **System Performance in MFLOP/sec**

System Performance = Number of Floating Point Operations/Wall-clock time

From old system performance in program A

System Performance in program A = Number of Floating Point Operations\*106/Wall-clock time in program A

Number of Floating Point Operations\*106 = System Performance in program A\* Wall-clock time in program A

Number of Floating Point Operations = (10\*4)/106 = 4\*10-5 MFLOP

For new system performance after the processor being replaced

New system performance = Number of Floating Point Operations\*106/Wall-clock time after the processor being replaced

New system performance = 4\*10-5 MFLOP/1.5seconds = 26.67MFLOP/sec

The new system performance after the processor being replaced is 26.67MFLOP/sec

**Question 2.**

You are on the design team for a new processor. The clock of the processor runs at 200 MHz. The following table gives instruction frequencies for Benchmark B, as well as how many cycles the instructions take, for the different classes of instructions. For this problem, we assume that (unlike many of today's computers) the processor only executes one instruction at a time.

|  |  |  |
| --- | --- | --- |
| Instruction Type | Frequency | Cycles |
| Loads & Stores | 30% | 6 cycles |
| Arithmetic Instructions | 50% | 4 cycles |
| All Others | 20% | 3 cycles |

* Calculate the CPI for Benchmark B.
* The CPU execution time on the benchmark is exactly 11 seconds. What is the ``native MIPS'' processor speed for the benchmark in millions of instructions per second?
* The hardware expert says that if you double the number of registers, the cycle time must be increased by 20%. What would the new clock speed be (in MHz)?
* The compiler expert says that if you double the number of registers, then the compiler will generate code that requires only half the number of Loads & Stores. What would the new CPI be on the benchmark?

**Solution**

* **Given**

From the box given above, it indicates number of clock cycles and their respective frequency

CPI (Cycle Per Instruction) = number of clock cycle \* frequency

CPI = 30/100\*6 + 50/100\*4 + 20/100\*3

CPI = 4.4 cycles per instruction

The CPI for Benchmark B is 4.4 cycles per instruction

* **Given**

CPU execution time = 11sec

Clock rate = 200MHz

Native MIPS processor speed?

MIPS (Millions of Instruction Per Second)

MIPS = frequency of the processor or clock rate/CPI\*106

MIPS = 200\*106/4.4\*106

MIPS = 45.45

The processor speed for the benchmark in millions of instructions per second is 45.45

* **Given**

From cycle time is inversely proportional to clock time

Cycle time = 1/clock rate

Cycle time = 1/200\*106

Cycle time = 5\*10-9

But from the question the cycle time has increased by 20%(0.2) so its 1+0.2=1.2

Cycle time = 5\*10-9 \*1.2

Cycle time = 6\*10-9

To get the new clock rate after being increased by 20%

New clock rate = 1/cycle time

New clock rate = 1/6\*10-9 = 166.667\*106 or166.667MHz

The new clock speed is 166.667MHz

* **Given**

The number of Loads & Stores is 30% but from the question it only needs half of the number of Loads & Stores that is 15%

Since before the number of registers was doubled the frequency of the instructions had a total 0f 100% but since 15% has been reduced from it, the total now becomes 85%

That is:

New CPI (Cycle Per Instruction) = number of clock cycle \* frequency

New CPI (Cycle Per Instruction) = 15/85\*6 + 50/85\*4 + 20/85\*3

New CPI (Cycle Per Instruction) = 4.12 cycles per instruction

The new CPI be on the benchmark is 4.12 cycles per instruction